REMARKS

Claims 1 - 45 are pending in the present application.

Applicant is amending claim 23 to clarify a feature of claim 23 that is neither disclosed nor suggested by the art of record. The amendment to claim 23 is not being made in response to a substantive rejection, and therefore Applicant submits that the doctrine of equivalents should be available for all of the elements of claim 23.

On 17 MAR 2005, Applicant submitted an Information Disclosure Statement (IDS). With the IDS, Applicant included a PTO-1449 that listed (a) a U.S. patent, and (b) an English translation of a formerly submitted German patent. The Office Action is accompanied by a copy of the PTO-1449 showing that the Office considered the U.S. patent, but it does not show that the Office considered the English translation of the German patent. Applicant respectfully requests that with the next communication, the Office include **a copy of the PTO-1449 showing that the Office considered the English translation of the German patent**.

Section 1 of the Office Action requires a new title. Applicant is amending the specification to provide a new title.

In section 3 of the Office Action, claims 1, 2, 4 – 9, 11, 13, 14, 16 – 23 and 25 – 30 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,262,871 to Wilder (hereinafter "the Wilder patent"). Applicant is traversing this rejection.

Claim 1 provides for a circuit. The circuit includes a decoder for receiving an address within an address space of a processor and for accessing a pixel in an active pixel sensor array based on the address. The decoder maps the active pixel sensor array to the address space.

The Wilder et al. patent, in FIG. 1, discloses a system that includes a row decoder 12, a column decoder 14, an image sensor 10, and a processor/computer 18. Image sensor 10 is arranged in 512 rows and 512 columns (col. 5, lines 25 – 27). Processor/computer 18 produces

supervisory signals that are applied to row decoder 12 and column detector 14 (col. 4, lines 54 – 56). The supervisory signals include address signals (col. 5, lines 2 – 3). Row decoder 12 is responsive to address inputs Bi applied via a bus 23 (col. 5, lines 44 – 45). Column decoder 14 is responsive to address inputs Aj applied via a bus 21 (col. 5, lines 49 – 50). The Wilder et al. patent states, at col. 5, lines 55 – 64:

> Each one of row decoder 12 and column decoder 14 is a decoder of the type which can decode "n" (e.g., 9) address inputs (Aj and Bi) to produce 2n (e.g., 512) unique decoded outputs. By varying the address inputs (Aj's and Bi's) and control inputs (Cj,s and Di,s) to decoder 12 and 14, as described hereinafter, the row decoder 12 and the column decoder 14 can be used to selectively energize, at any one time, one or more of the 512 row conductors or one or more of the 512 column conductors of the sensor 10. (emphasis added)

Note that $2^9 = 512$. Therefore, the nine address inputs Aj represent a column address between 0 and 511, to designate one of the 512 columns of image sensor 10 (col. 7, lines 12 – 16). Similarly, the nine address inputs Bi represent a row address between 0 and 511, to designate one of the 512 rows of image sensor 10. Thus, the address provided to column decoder 14 is a column address, and the address provided to row decoder 12 is a row address. FIG. 2 expressly identifies these addresses as a row address and a column address.

In the Wilder et al. patent, the address provided to column decoder 14 is a column address, and the address provided to row decoder 12 is a row address. Thus, processor/computer 18 apparently calculates each of the column address and the row address, and as such, column decoder 14 and row decoder 12 do not receive an address within an address space of processor/computer 18. Consequently, the Wilder et al. patent does not disclose either of (a) a decoder for receiving **an address within an address space of a processor** and for accessing a pixel in an active pixel sensor array based on said address, or (b) wherein said decoder maps said active pixel sensor array **to said address space** [of said microprocessor], both of which are recited in claim 1. Thus, the Wilder et al. patent does not anticipate claim 1.

Claims 2 and 4 – 9 depend from claim 1. By virtue of this dependence, claims 2 and 4 – 9 are also novel over the Wilder et al. patent.

Claim 11 is an independent claim, and includes a recital similar to that of claim 1, as described above. For reasoning similar to that provided in support of claim 1, the Wilder et al. patent does not anticipate claim 11.

Claims 13, 14 and 16 – 21 depend from claim 11. By virtue of this dependence, claims 13, 14 and 16 – 21 are also novel over the Wilder et al. patent.

Claim 22 provides an interface. The interface includes a module that enables a processor to access a pixel circuit in an active pixel sensor array by direct memory access.

FIG. 1 of the present application shows an exemplary embodiment of an interface, i.e., RAIS 100, in accordance with claim 22. RAIS 100 enables a microprocessor 3 to address a pixel matrix 2 from within the memory space of microprocessor 3, as microprocessor 3 does with any other peripheral, that is, by direct memory access.

As mentioned above during the discussion of claim 1, in the Wilder et al. patent, the address provided to column decoder 14 is a column address, the address provided to row decoder 12 is a row address, and processor/computer 18 apparently calculates each of the column address and the row address. Column decoder 14 and row decoder 12 do not receive an address within an address space of processor/computer 18 and so, the Wilder et al. patent does not disclose a module that enables a processor to access a pixel circuit in an active pixel sensor array by **direct memory access**, as recited in claim 22. Consequently, the Widler et al. patent does not anticipate claim 22.

Claims 23 and 25 – 30 depend from claim 22. By virtue of this dependence, claims 23 and 25 – 30 are also novel over the Wilder et al. patent.

Applicant respectfully requests reconsideration and withdrawal of the section 102(b) rejection set forth in section 3 of the Office Action.

In section 4 of the Office Action, claims 22 and 26 – 29 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,512,218 to Canini et al. (hereinafter "the Canini et al. patent"). Applicant is traversing this rejection.

The Canini et al. patent, in FIG. 6, discloses a system that includes a CMOS sensor 5, a microprocessor 15, a logic control unit 10, and a RAM memory 17. CMOS sensor 5 is a matrix of pixels (col. 3, lines 20 – 23). Microprocessor 15 is connected to logic control unit 10, and supplies control signals to logic control unit 10 for acquiring signals associated with the pixels (col. 3, lines 59 – 64). DMA controller 30 is for furnishing available digital image data to microprocessor 15, by transferring it directly to RAM memory 17 (col. 5, lines 52 – 55). The Canini et al. patent, states, at col. 5, lines 55 – 60:

> In particular, when the image must be transferred to RAM memory 17, the DMA controller 30 requests the microprocessor 15 for control of the data bus 33, via the control line 32 and when it obtains this control, it generates the addresses and the control signals necessary to store the output image of A/D converter 7 directly in RAM memory 17. (emphasis added)

In the Canini et al. patent, microprocessor 15 supplies control signals to logic control unit 10. There is no suggestion that the control signals provide an address in the address space of microprocessor 15, and so microprocessor 15 does not access either of control unit 10 or CMOS sensor 5 by direct memory access. Furthermore, DMA controller 30 is for transferring image data to RAM memory 17, and there is no mention of DMA controller enabling microprocessor 15 to access CMOS sensor 5. Consequently, the Canini et al. patent does not disclose a module that enables a **processor to access a pixel circuit** in an active pixel sensor array by **direct memory access**, as recited in claim 22.

Claims 26 – 29 depend from claim 22. By virtue of this dependence, claim 26 – 29 are also novel over the Canini et al. patent.

Applicant respectfully requests reconsideration and withdrawal of the section 102(e) rejection set forth in section 4 of the Office Action.

In section 5 of the Office Action, claims 22 and 25 – 29 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication No. 2002/0074481 to McGrath et al. (hereinafter "the McGrath et al. publication"). Applicant is traversing this rejection.

The McGrath et al. publication, in FIG. 5, discloses a system that includes an image acquisition die 117, a DMA 173, and a microcontroller 150. The McGrath et al. publication states, in par. 30:

> The image acquisition die is connected to the control bus 144 via the line 154 and to the data bus 142 via lines 176 and 175. Signal lines 123 and 124 provide the signals between the image acquisition die 117 and the DMA 173, and the address signals are provided to the address bus 143 via line 174. (emphasis added)

Apparently, address signals are provided from DMA 173 to address bus 143, which is consistent with DMA 173 taking control of address bus 143 in order to transfer data from image acquisition die 117 to a memory device, such as, for example, DRAM 190 (see FIG. 5). The McGrath et al. publication does not further mention DMA 173, and in particular, the McGrath et al. publication does not disclose that DMA 173 operates to enable microcontroller 150 to access image acquisition die 117 by direct memory access. Applicant respectfully requests that if the Examiner asserts that the McGrath et al. publication discloses that DMA 173 operates to enable microcontroller 150 to access image acquisition die 117 by direct memory access, that the Examiner **please provide a citation to a passage of the McGrath et al. publication** in support of such assertion. Absent such a disclosure, Applicant submits that the McGrath et al. publication does not disclose a module that enables **a processor to access a pixel circuit** in an active pixel sensor array **by direct memory access**, as recited in claim 22. Thus, the McGrath et al. publication does not anticipate claim 22.

Claims 25 – 29 depend from claim 22. By virtue of this dependence, claims 25 – 29 are also novel over the McGrath et al. publication.

Applicant respectfully requests reconsideration and withdrawal of the section 102(e) rejection set forth in section 5 of the Office Action.

In section 7 of the Office Action, claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Canini et al. patent. Applicant is traversing this rejection.

Claims 24 and 25 depend from claim 22. Above, Applicant explained that the Canini et al. patent does not disclose a module that enables a processor to access a pixel circuit in an active pixel sensor array by direct memory access, as recited in claim 22. Accordingly, Applicant submits that claim 22 is patentable over the Canini et al. patent. Claims 24 and 25, by virtue of their dependence on claim 22, are also patentable over the Canini et al. patent.

Applicant respectfully requests reconsideration and withdrawal of the section 103(a) rejection set forth in section 7 of the Office Action.

In section 8 of the Office Action, claims 3, 12, 15, 32 – 39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Wilder et al. patent in view of the Canini et al. patent. Applicant is traversing this rejection.

Claim 3 depends from claim 1, and claims 12 and 15 depend from claim 11. Above, Applicant explained that the Wilder et al. patent does not disclose certain features of claims 1 and 11. Applicant submits that the Canini et al. patent does not make up for the deficiency of the Wilder et al. patent, as the Wilder et al. patent relates to claims 1 and 11. Thus, claims 1 and 11, and claims 3, 12 and 15, by virtue of their dependencies, are all patentable over the cited combination of the Wilder et al. and Canini et al. patents.

Claim 32 is an independent claim that provides for a system. The system includes, *inter alia*, a decoder for accessing a pixel of an active pixel sensor array based on an address, wherein the address is within an address space of a microprocessor, and wherein the decoder maps the active pixel sensor array to the address space. Thus, claim 32 includes a recital similar to that of

claim 1, as described above. As such, claim 32, for reasoning similar to that provided in support of claim 1, is patentable over the cited combination of the Wilder et al. and Canini et al. patents.

Claims 33 – 39 and 42 depend from claim 32. By virtue of this dependence, claims 33 – 39 and 42 are also patentable over the cited combination of the Wilder et al. and Canini et al. patents.

Applicant respectfully requests reconsideration and withdrawal of the section 103(a) rejection set forth in section 8 of the Office Action.

In section 9 of the Office Action, claims 10 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Wilder et al. patent in view of U.S. Patent No. 5,296,852 to Rathi et al. (hereinafter "the Rathi et al. patent"). Applicant is traversing this rejection.

Claim 10 depends from claim 1, and claim 31 depends from claim 22. Above, Applicant explained that claims 1 and 22 are novel over the Wilder et al. patent. The Rathi et al. patent does not make up for the deficiency of the Wilder et al. patent as the Wilder et al. patent relates to claims 1 and 22. Thus, claims 1 and 22, and claims 10 and 31, by virtue of their dependencies, are all patentable over the cited combination of the Wilder et al. and Rathi et al. patents.

Applicant respectfully requests reconsideration and withdrawal of the section 103(a) rejection set forth in section 9 of the Office Action.

In section 6 of the Office Action, claims 41 and 43 – 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Wilder et al. patent, in view of the Canini et al. patent and U.S. Patent No. 6,825,936 to Metcalfe et al. (hereinafter "the Metclafe et al. patent"). During an informal telephone conversation between Applicant and Examiner Luu on 14 NOV 2005, Examiner Luu clarified that claim 40 is also being rejected. Thus, Applicant is addressing the rejection of claims 40, 41 and 43 – 45. Nevertheless, Applicant is traversing this rejection.

Claims 40, 41 and 43 – 45 depend from claim 32. Above, Applicant explained that claim 32 is patentable over the cited combination of the Wilder et al. and Canini et al. patents. Applicant submits that the Metcalfe et al. patent does not make up for the deficiency of the cited combination of the Wilder et al. and Canini et al. patents, as the combination relates to claim 32. Thus, claim 32, and claims 40, 41 and 43 – 45, by virtue of their dependence on claim 32, are all patentable over the cited combination of the Wilder et al., Canini et al. and Metcalfe et al. patents.

Applicant respectfully requests reconsideration and withdrawal of the section 103(a) rejection set forth in section 10 of the Office Action.

In view of the foregoing, Applicant respectfully submits that all claims presented in this application patentably distinguish over the prior art. Accordingly, Applicant respectfully requests favorable consideration and that this application be passed to allowance.

Respectfully submitted,

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Date

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